Remarks

Claims 1, 2, 4, 6-10 and 12-16 are pending in the application. Claims 1, 2, 4, 6, 8-10 and 12-16 stand rejected, while claim 7 is objected to. By this response, claims 1 and 6 are amended, claim 7 is canceled and new claim 17 has been added. Applicants respectfully request that claims 1, 2, 4, 6, 8-10 and 12-17 be passed to issuance.

Claim Objections

The Examiner objected to claim 7 as being dependent upon a rejected base claim, but indicated claim 7 would be allowable if rewritten in independent from including all the limitations of the base claim and any intervening claims. Applicants have amended independent claim 6 to include the limitations of dependent claim 7, therefore claim 6 is allowable.

Claim Rejections - 35 U.S.C. § 102(b)

The Examiner rejected claims 16 under 35 U.S.C. § 102(b) as being anticipated by U.S Patent Application No. 20020064075 to Morishima. The Examiner stated that Morishima discloses a computer system memory in which simultaneous switching noise is reduced by inverting signals based on a selected operation mode. The Examiner cited ¶ 0047 of the Summary of the Invention, which references a prior art DRAM memory having a bit twisting structure known as "pseudo two intersection point memory cell."

Applicants respectfully submit that Morishima is directed to a memory system where adjacent bitlines are not read simultaneously, which in turn reduces capacitive coupling between adjacent bit lines during read operations. "By maintaining the unselected bit line on the adjacent columns in the precharged state, this unselected bit line can be utilized as a shield layer, and the inter-bit-line interference can be reliably suppressed." (Morishima at ¶ 51-53 and 92-95) Applicants respectfully submit that Morishima does not disclose a memory system capable of receiving either non-inverted or inverted signals, nor does it disclose external re-drive circuitry to

selectively output non-inverted or inverted outputs.

In Figs. 1-3, cited by the Examiner, Morishima discloses a precharge control circuit internal to the memory device, where odd numbered bit lines (columns) and even numbered bit lines (columns) are precharged to different levels, i.e. the signal for the odd numbered columns is disabled while the signal for the even numbered columns is enabled. ("Thus, when column address signal Y0 is at L level, and designates the odd-numbered columns, precharge signal /PC 1 for the bit line load circuits provided for the odd-numbered columns is deactivated. In this case, precharge signal /PC 2 for the bit line load circuits L2 and L4 of the even numbered columns maintain L level, and the bit lines in these even-numbered columns maintain the precharged state." Morishima at ¶ 101, see ¶¶ 100-103.) The precharge control circuit of Morishima is internal to the memory device and is used to ensure that adjacent bit lines are placed in opposing states to reduce capacitive coupling and thereby allow faster read access. (See ¶ 0092 of Morishima) Accordingly, Morishima does not anticipate Applicants' memory system which is directed toward reducing simultaneous switching noise through the use of re-drive circuitry to provide both non-inverted and inverted address/command polarities to the SDRAMs. (Applicants' Specification at ¶ 0012) Applicants' memory system "reduces the maximum count of drivers that will be switching in any one direction at a time, by utilizing a memory device that is designed to accept inverted inputs when so programmed." (Applicants' Specification at ¶ 0025)

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. (MPEP §2131) Applicants respectfully submit that Morishima does not teach or suggest Applicants' claimed memory system in which a memory controller responsive to a programmable pin directs selected banks of the memory to accept either a non-inverting or an inverting input to reduce simultaneous switching noise. (Applicants' Specification at Paragraph 22) Indeed, there is no teaching in Morishima regarding modulating the logic polarity of selected memory bank inputs. Accordingly, Applicants respectfully submit that Morishima does not anticipate the memory system claimed herein and therefore the Examiner's rejection of claim 16 under 35 U.S.C. § 102(b) has been overcome.

Claim Rejections - 35 U.S.C. § 103(a)

The Examiner rejected claims 1, 2, 4, 6, 8-10 and 12-15 under 35 U.S.C. § 103(a) a being unpatentable over U.S. Patent No. 5,513,135 to Dell in view of U.S. Patent No. 5,999,483 to Itou. The Examiner stated that Dell discloses a memory system with a plurality of DRAMs while Itou discloses a circuit capable of accepting non-inverted and inverted inputs along with a programmable register to enable operation of the memory in either mode. The Examiner stated it would have been obvious to person of ordinary skill in the art to modify the memory circuit of Dell to include the programmable elements of Itou, since the modification would be merely a substitution of functionally recognized equivalent elements.

Applicants respectfully submit that Itou teaches an internal structure and operation of a synchronous memory device where the drive strength of the output buffers may be varied, based on a current operating frequency of the memory device. ("The control circuit controls the output buffer circuit in accordance with the frequency of the clock signal to change the current supplying capability of the transistor element." Itou at Col. 2:4-7) Figures 1 and 2 of Itou illustrate the receipt of inputs to the memory via an address buffer 14 and control signal buffer 16. The input signals are used to set the mode register for the memory using clocked inverters 133 and latches 134. Once the mode register is set, the output buffer transistors can be selectively activated, such that fewer transistors are selected at lower frequencies, thereby slowing output transitions at lower frequency operation, as is required by industry specifications. (See Abstract and Col. 6:36-67 through Col. 7:1-29 of Itou). The non-inverting and inverting inputs of Itou merely relate to the setting of various mode address bits used to set clock frequency, which then determines the number of transistors activated in the output buffer of Itou's memory system. (Figs. 1 and 2 of Itou)

Accordingly, Itou does not teach or suggest Applicants' claimed memory system in which a memory controller responsive to a programmable pin directs selected banks of the memory system to vary the polarity of the signals propagated to the memory devices to reduce simultaneous switching noise.

Applicants respectfully submit that Dell discloses a memory module which may include synchronous memory devices, decoupling capacitors and registers. Since Itou discloses a fundamentally different structure and application then claimed herein, no motivation is seen to combine Itou with Dell, and, in any case, neither reference, either taken singularly or in combination teach Applicants' claimed memory system. Applicants therefore respectfully submit that Applicants' memory system cannot be implemented by a mere substitution of a functionally recognized equivalent as suggested and that the Examiner's rejection of claims 1, 2, 4, 6, 8-10 and 12-15 under 35 U.S.C. § 103(a) has been overcome.

Prior Art Made of Record

The prior art made of record by the Examiner and not relied upon, i.e. Arimuto (U.S. Patent No. 5,612,919), Ochoa, et al. (U.S. No. Patent 6,347,394), Takahashi et al. (U.S. Patent Application No. 2003/0112668), and Penchuk (U.S. Patent No. 7,145,819) have been reviewed and Applicant respectfully submits that the references cited do not anticipate or suggest the elements of the pending claims.

Conclusion

Based on the foregoing, it is respectfully submitted the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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